Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A method of fabricating a memory cell array in which memory cells formed of ferroelectric capacitors are arranged in a matrix, ~~comprising the steps of:~~comprising:

forming a first signal electrode with a predetermined pattern on a base;

selectively forming a ferroelectric layer on the first signal electrode linearly along the first signal electrode; ~~and~~

forming a dielectric layer between laminates each of which includes the first signal electrode and the ferroelectric layer so as to cover an exposed surface of the base;

planarizing the dielectric layer so as to have a surface at the same level as the ferroelectric layer after forming the dielectric layer; and

forming a second signal electrode in a direction intersecting the first signal electrode.

2. (Currently Amended) The method of fabricating a memory cell array as defined in claim 1, further ~~comprising the steps of:~~ comprising:

forming on the base a first region having surface properties which give priority in deposition to a material of at least one of the first signal electrode and the ferroelectric layer, and a second region having surface properties which give difficulty in deposition to the material of at least one of the first signal electrode and the ferroelectric layer in comparison with the first region; and

providing the material of at least one of the first signal electrode and the ferroelectric layer and selectively forming one of the first signal electrode and the ferroelectric layer in the first region.

3. (Original) The method of fabricating a memory cell array as defined in claim 2,

wherein the first and second regions are defined on a surface of the base.

4. (Original) The method of fabricating a memory cell array as defined in claim 3, wherein:

the surface of the base is exposed in the first region; and

in the second region is formed an undercoat layer having surface properties having a low affinity for materials of the first signal electrode and the ferroelectric layer in comparison with the exposed surface of the base in the first region.

5. (Original) The method of fabricating a memory cell array as defined in claim 3, wherein:

the surface of the base is exposed in the second region; and

in the first region is formed an undercoat layer having surface properties having a high affinity for materials of the first signal electrode and the ferroelectric layer in comparison with the exposed surface of the base in the second region.

6. (Canceled).

7. (Currently Amended) The method of fabricating a memory cell array as defined in ~~claim 6,~~ claim 1,

wherein the dielectric layer is formed of a material having a dielectric constant lower than a dielectric constant of the ferroelectric layer.

8. (Currently Amended) A method of fabricating a memory cell array in which memory cells formed of ferroelectric capacitors are arranged in a matrix, ~~comprising the steps of:~~ comprising:

forming a first signal electrode with a predetermined pattern on a base; ~~and~~

forming a ferroelectric layer and a second signal electrode in a direction intersecting the first signal electrode, wherein the ferroelectric layer is disposed linearly along the second signal ~~electrode.~~ electrode;

forming a dielectric layer between laminates each of which includes the second signal electrode and the ferroelectric layer so as to cover an exposed surface of the base and an exposed surface of the first signal electrode; and

planarizing the dielectric layer so as to have a surface at the same level as the second signal electrode after forming the dielectric layer.

9. (Original) The method of fabricating a memory cell array as defined in claim 8,

wherein the ferroelectric layer and the second signal electrode are patterned by etching using the same mask.

10. (Canceled).

11. (Currently Amended) The method of fabricating a memory cell array as defined in ~~claim 10,~~ claim 8,

wherein the dielectric layer is formed of a material having a dielectric constant lower than a dielectric constant of the ferroelectric layer.

12. (Currently Amended) A method of fabricating a memory cell array in which memory cells formed of ferroelectric capacitors are arranged in a matrix, ~~comprising the steps of:~~comprising:

forming a first signal electrode with a predetermined pattern on a base;

forming a ferroelectric layer on the first signal electrode linearly along the first signal electrode;

patterning the ferroelectric layer to be disposed only in an intersection area of the first and second signal electrodes;

forming a dielectric layer between laminates each of which includes the first signal electrode and the ferroelectric layer so as to cover an exposed surface of the base;

planarizing the dielectric layer so as to have a surface at the same level as the ferroelectric layer after forming the dielectric layer; and

forming a second signal electrode in a direction intersecting the first signal ~~electrode; and~~

~~patterning the ferroelectric layer to be disposed only in an intersection area of the first and second signal electrodes.~~electrode.

13. (Currently Amended) The method of fabricating a memory cell array as defined in claim 12, further ~~comprising the steps of:~~ comprising:

forming on the base a first region having surface properties which give priority in deposition to a material of at least one of the first signal electrode and the ferroelectric layer, and a second region having surface properties which give difficulty in deposition to the material of at least one of the first signal electrode and the ferroelectric layer in comparison with the first region; and

providing the material of at least one of the first signal electrode and the ferroelectric layer and selectively forming one of the first signal electrode and the ferroelectric layer in the first region.

14. (Original) The method of fabricating a memory cell array as defined in claim 13,

wherein the first and second regions are formed on a surface of the base.

15. (Original) The method of fabricating a memory cell array as defined in claim 14, wherein:

part of the surface of the base is exposed in the first region; and

in the second region is formed an undercoat layer having surface properties having a low affinity for materials of the first signal electrode and the ferroelectric layer in comparison with the exposed surface of the base in the first region.

16. (Original) The method of fabricating a memory cell array as defined in claim 14, wherein:

part of the surface of the base is exposed in the second region; and

in the first region is formed an undercoat layer having surface properties having a high affinity for materials of the first signal electrode and the ferroelectric layer in comparison with the exposed surface of the base in the second region.

17. (Original) The method of fabricating a memory cell array as defined in claim 12,

wherein the ferroelectric layer and the second signal electrode are patterned by etching using the same mask.

18. (Canceled).

19. (Original) The method of fabricating a memory cell array as defined in claim 18,

wherein the dielectric layer is provided between laminates each of which includes the second signal electrode and the ferroelectric layer so as to cover the exposed surface of the base and an exposed surface of the first signal electrode.

20. (Original) The method of fabricating a memory cell array as defined in claim 18,

wherein the dielectric layer is formed of a material having a dielectric constant lower than a dielectric constant of the ferroelectric layer.